IN THE CLAIMS:

Please amend claims 6, 22-23, and 29 as follows:

1. (Previously Amended) A method of manufacturing thin film transistors comprising the steps of:

(a) forming a plurality of island-shaped semiconductor layers on a substrate having an insulative surface;

(i) forming a gate insulating film on and across an intermediate region of each of the semiconductor layers, the gate insulating film having a thickness not larger than 50 nm, and exposing end regions of each of the semiconductor layers;

(ii) forming a gate electrode on the gate insulating film over each of said semiconductor layers, the gate electrode being retarded from edges of the gate insulating film, defining in each of the semiconductor layers a channel region below the gate electrode, and a pair of offset regions below the gate insulating film between the channel region and the end regions;

(b) implanting dopant into the offset regions in each of said semiconductor layers through the gate insulation film by ion implantation to form lightly doped regions; and

(c) implanting dopant into the end regions in each of said semiconductor layers directly to form heavily doped source/drain regions whose impurity concentration is higher than that of said lightly doped regions,

wherein said ion implanting steps (b) and (c) are so selected that hydrogen ions are also implanted into said lightly doped regions and said heavily doped source/drain regions, but not into said channel region under said gate electrode.

2. (Original) The method of manufacturing the thin film transistors according to claim 1, wherein said ion implanting steps (b) and (c) are carried out using an apparatus for non-mass-analyzed ion implantation which uses an ion source comprising a filament which emits thermal electrons.

3. (Previously Amended) The method of manufacturing the thin film transistors according to claim 2, wherein said ion implanting steps (b) and (c) are carried out with acceleration energy equal to less than 30 keV.

4. (Original) The method of manufacturing the thin film transistors according to claim 2, wherein said ion implanting steps (b) and (c) are carried out using a hydride of a dopant element as an ion source.

5. (Previously Amended) The method of manufacturing the thin film transistors according to claim 1, wherein said step (a) comprises the substeps of:

(a-1) depositing an amorphous semiconductor layer on said substrate;

and

(a-2) irradiating a laser beam on said amorphous semiconductor layer, to change said amorphous semiconductor layer into a crystalline semiconductor layer.

6. (Currently Amended) The method of manufacturing the thin film transistors according to claim 3, further comprising the step of:

(d) after said step (c), irradiating a laser beam onto said lightly doped regions through a thin insulation film and said source/drain regions ~~through said thin insulation film~~ directly to activate impurities and recover damages caused by the ion implantation.

7-21. (Withdrawn)

22. (Currently Amended) A method of manufacturing thin film transistors comprising the steps of:

(a) forming a plurality of island-shaped semiconductor layers on a substrate having an insulative surface;

(i) forming a gate insulating film on and across an intermediate region of said substrate, said film covering at least a portion of said semiconductor layers, the gate insulating film having a thickness not larger than 50 nm, and exposing end regions of each of the semiconductor layers;

(ii) forming a gate electrode layer on said gate insulating film, the gate electrode being retarded from edges of the gate insulating film, defining in each of the

semiconductor layers a channel region below the gate electrode, and a pair of offset regions below the gate insulating film between the channel region and the end regions;

(b) implanting dopant into the offset regions in each of said semiconductor layers through the gate insulation film by ion implantation to form lightly doped regions;

(c) implanting dopant into the end regions in each of said semiconductor layers directly to form heavily doped source/drain regions whose impurity concentration is higher than that of said lightly doped regions; and

(d) irradiating a laser beam ~~directly or~~ through said gate insulation film to said source/drain regions and said offset regions to activate dopants implanted in steps (b) and (c).

23. (Currently Amended) A method of manufacturing thin film transistors having a channel region, offset regions, lightly doped regions, and heavily doped source/drain regions, comprising the steps of:

(a) forming a plurality of island-shaped semiconductor layers on a substrate having an insulative surface;

(i) forming a gate insulating film on each of said semiconductor layers;

(ii) forming a gate electrode on said gate insulating film over each of said semiconductor layers, the gate electrode being retarded from the edges of the gate

insulating film to define in the semiconductor layer, the channel region below the gate electrode, and the offset regions adjacent to the channel region under the gate insulating film;

(b) implanting dopant into first regions ~~under~~ of the semiconductor layer outside of said gate insulating film, ~~at outsides of regions designated for the offset regions, and adjacent to the channel region under said gate electrode in each of said semiconductor layers~~ directly by ion implantation to form the lightly doped regions; and

(c) implanting dopant into outer regions within said first regions in each of said semiconductor layers directly to form the heavily doped source/drain regions whose impurity concentration is higher than that of the lightly doped regions,

wherein said ion implanting steps (b) and (c) are so selected that hydrogen ions are also implanted into the lightly doped regions and the heavily doped source/drain regions, but not into the channel region under said gate electrode, and

wherein said dopant cannot substantially be implanted into the ~~offset regions~~ channel region.

24. (Previously Added) The method of manufacturing thin film transistors according to claim 23, wherein said ion implanting steps (b) and (c) are carried out using an apparatus for non-mass-analyzed ion implantation which uses an ion source comprising a filament which emits thermal electrons.

25. (Previously Added) The method of manufacturing thin film transistors according to claim 24, wherein said ion implanting steps (b) and (c) are carried out with acceleration energy less than or equal to 30ke V.

26. (Previously Added) The method of manufacturing thin film transistors according to claim 24, wherein said ion implanting steps (b) and (c) are carried out using a hydride of a dopant element as an ion source

27. (Previously Added) The method of manufacturing thin film transistors according to claim 23, wherein said step (a) further comprises the substeps of:

(a-1) depositing an amorphous semiconductor layer on said substrate; and

(a-2) irradiating a laser beam on said amorphous semiconductor layer, to change said amorphous semiconductor layer into a crystalline semiconductor layer.

28. (Previously Added) The method of manufacturing thin film transistors according to claim 25, further comprising the step of:

(d) after said step (c), irradiating a laser beam onto the lightly doped regions and the source/drain regions directly to activate impurities and recover damages caused by the ion implantation.

29. (Currently Amended) A method of manufacturing thin film transistors having a channel region, offset regions, lightly doped regions and heavily doped source/drain regions, comprising the steps of:

(a) forming a plurality of island-shaped semiconductor layers on a substrate having an insulative surface;

(i) forming a gate insulating film on said substrate, said film covering said semiconductor layers;

(ii) forming a gate electrode layer on said gate insulating film, the gate electrode layer being retarded from edges of said gate insulating film;

(b) implanting dopant into first regions, at outsides of said gate insulating film and regions designated for the offset regions under said gate insulating film, ~~and~~ which are adjacent to the channel region below a gate electrode, in each of said semiconductor layers directly by ion implantation to form the lightly doped regions;

(c) implanting dopant into outer regions within said first regions in each of said semiconductor layers directly to form the heavily doped source/drain regions whose impurity concentration is higher than that of the lightly doped regions; and

(d) irradiating a laser beam directly ~~or through said thin insulation film~~ to said first regions to activate dopants implanted in steps (b) and (c),

wherein said dopant cannot substantially be implanted into ~~said offset regions~~ the channel region.